Remarks

Applicant respectfully requests reconsideration of this application as amended. No claims have been amended. No claims have been cancelled. Therefore, claims 1-5, 7-16, 18-27 and 29-33 are presented for examination.

Claims 1-5, 7-16, 18-27, and 29-33 stand rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. Applicant submits that the present claims are in conformance with 35 U.S.C. §101, and thus are in proper condition for allowance.

35 U.S.C. §101 permits patents to be granted only for "*any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof.*" The term "process" as defined in 35 U.S.C. 100, means process, art or method, and includes a new use of a known process, machine, manufacture, composition of matter, or material. MPEP § 706.03. Moreover, the Examiner maintains that "in order for claims to be statutory, claims must include a practical/physical application **or** a concrete, useful and tangible result. See Office Action at Page 2, paragraph 4.

The claims of the present application clearly include statutory subject matter comprising a **practical/physical application.** For instance, each of the claims recites processes implemented by an execution unit and other components within a processor. Applicant submits that the claiming of novel processes involving hardware components of a processor is both practical and physical. Accordingly, the present claims are properly directed to statutory subject matter.

Claims 1-5, 7-8, 10-16, 18-19, 21-27, 29, and 31-33 stand rejected under 35 U.S.C. §102(e) as being anticipated by Sih et al. (U.S. Patent No. 6,606,700). Applicant submits that the present claims are patentable over Sih.

Sih discloses a digital signal processor architecture that is designed to speed up frequently-used signal processing computations, such as FIR filters, correlations, FFTs, and DFTs. The architecture uses a coupled dual-MAC architecture and attaches a dual-MAC coprocessor onto it in such a way as to achieve an increase in processor capability. (Sih at col. 1, ll. 49-55.)

Claim 1 of the present application recites saving input data at one or more buffers within an execution unit for one or more multiply-accumulate operations to be performed during a subsequent computational cycle. Applicant submits that nowhere in Sih is there disclosed, or reasonably suggested, an *execution unit* ***having buffers to save data*** *to perform multiply-accumulate operations* ***during a subsequent computational cycle.***

The Examiner maintains that buffers IS1 122 and IS2 138 in Figure 1 of Sih discloses buffers that save data to perform multiply-accumulate operations during a subsequent computational cycle. See Office Action at Page 4 at first full paragraph. However, Sih discloses that IS1 122 and IS2 138 receive outputs, directly or indirectly, from a register file. There is *no disclosure, or reasonable suggestion, of these elements being* ***located within an execution unit*** *to store* ***input data received at the execution***.

Further, there is no disclosure of values stored within IS1 122 and IS2 138 being *saved for use at the execution* ***to perform multiply-accumulate operations during a subsequent computational cycle***. Particularly, based upon the number of functional elements (e.g., Mixes, multipliers, shifters, etc.) between the storage elements and the MAC

components, it is highly unlikely that values stored in the storage elements could be used at MAC3 or MAC4 during a subsequent computational cycle. For the foregoing reasons, claim 1, and its dependent claims, is patentable over Sih.

Independent claims 10 and 21 include limitations similar to those recited in claim 1. Therefore, claims 10 and 21, as well as their respective dependent claims, are also patentable over Sih for the reasons discussed above with respect to claim 1.

Claims 9, 20, and 30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sih et al. (U.S. Patent No. 6,606,700). in view of Agarwal et al. (U.S. Patent No. 5,825,677). Applicant submits that the present claims are patentable over Sih even in view of Agarwal. Agarwal does not remedy the deficiencies of Sih as far as disclosing the claims of the present application. As a result, the present claims are also patentable over Sih, even in view of Agarwal.

Applicant submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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